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Question Paper Code : 50426

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023

Fourth/Fifth/Seventh Semester

Computer Science and Engineering

CS 8491 – COMPUTER ARCHITECTURE

(Common to Computer and Communication Engineering / Electrical and Electronics Engineering / Robotics and Automation/ Information Technology)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the functions of data path unit and control path unit.
2. What are the methods to improve system performance?
3. How many levels of 4-2 reducers are needed to reduce k summands to 2 in a reduction tree?
4. Give the subtraction rules for floating point numbers.
5. Why is single – cycle implementation not used in modern devices? Explain.
6. Give the importance of pipelining.
7. Sketch the architecture of MISD.
8. List the advantages of GPU.
9. Compare and contrast SRAM and DRAM.
10. Find the AMAT for a processor with 1 ns clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.25 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls.

PART B — (5 × 13 = 65 marks)

11. (a) Register R5 is used in a program to point to the top of a stack containing 32-bit numbers. Write a sequence of instructions using the Index. Autoincrement, and Autodecrement addressing modes to perform each of the following tasks;

(i) Pop the top two items off the stack, and them, then push the result onto the stack. (5)

(ii) Copy the fifth item from the top into register R3. (4)

(iii) Remove the top ten items from the stack. (4)

For each case, assume that the stack contains ten or more elements.

Or

(b) Multiply each of the following pairs of signed 2's- complement numbers using the Booth algorithm. In each case, assume that A is the multiplicand and B is the multiplier.

(i) A = 010111 and B = 110110 (4+1)

(ii) A = 110011 and B = 101100 (4)

(iii) A = 001111 and B = 001111 (4)

12. (a) Explain hardware implementation of floating – point operations with neat sketch.

Or

(b) (i) Draw the flowchart and explain about booth algorithm (6)

(ii) Multiply 100111 with 11011 using booths algorithm. (7)

13. (a) Explain basic MIPS implementation with neat diagram.

Or

(b) With neat diagram discuss data hazard and stalls.

14. (a) (i) Brief the difficulties in parallel processing. Explain how speed-up challenge is addressed with example. (7)

(ii) What are the performance metrics of parallel systems? (6)

Or

(b) Explain the flynn's classification of computer with suitable diagram.

15. (a) With neat sketch explain various mapping techniques of cache memory?

Or

(b) Define Interrupts. Explain how to interrupts from multiple devices in detail.

PART C — (1 × 15 = 15 marks)

16. (a) (i) Consider three processors P1, P2, and P3 executing same instruction set. P1 has 2 GHz of clock rate and CPI of 1.5. P2 has a 3.5 GHz clock rate and a CPI of 1.0. P3 has 3.0 GHz clock rate and has CPI of 2.2. Find which processor has the highest performance expressed in instructions per second. Also find the number of cycles and number of instructions in each processor if each processor executes a program in 10 seconds. (7)

(ii) Discuss DMA controller with neat block diagram? (8)

Or

(b) (i) Consider a two address format specified as source, destination. Examine the following sequence of instruction and explain the addressing modes used and the operations done in each instruction.

(1) MOVE (R3) +, R0 (2)

(2) ADD (R3) +, R0 (2)

(3) MOVE R0, (R3) (2)

(4) MOVE 8(R3), (R5) (2)

(5) ADD #70, R3 (2)

(ii) Compare and contrast fine grained multi-threading and coarse grained multi-threading? (5)